REMARKS

In the Office Action, the Examiner has objected to the drawings and the specification. The Examiner has also rejected claim 1 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement and claims 1-12 under 35 U.S.C. § 112, second paragraph, as being indefinite.

Pursuant to this Reply, claims 3, 4, 8, 10, and 11 are amended in accordance with the opinions of the esteemed Examiner regarding that the two transistors of circuit (312) are only the loads of the amplifier comprising elements (31), and to disclose the unique feature of the present invention that the circuit (312), renamed as "a shared active load", is shared by and electrically connected to the first differential receiving circuit (311) of the first differential comparator (31) and the renamed "main differential receiving circuit" (322) of the second differential receiving circuit (including elements: the renamed "pre-amplifier receiving circuit" 321, and 322) of the second differential comparator (32) so as to form a first operational amplifier (including elements 311, 312) and a second operational amplifier (including elements 322, 312) respectively. The contents of the specification are modified to cope with the esteemed Examiner's comments to label the transistors of Fig. 4, describe the voltage levels of the detected place "a", and replace the renamed terms. All the above-mentioned amendments of the claims, modifications of the specification and drawings that are employed to clarify the

contents of the present invention, either can find support in the claims, specification, and drawings as originally filed, or are known to one with the ordinary skill in the field, and do not contain any new matter.

The Examiner requested that the trigger signal and the stop signal be shown in Fig. 4 of the present invention and that the Applicants explain how the voltage ranges are detected. Accordingly, the Applicants offer the following. The trigger signal is produced by the detecting circuit as disclosed in claims 1, 8, and 12 as originally filed, and the stop signal is also produced by the detecting circuit as described on paragraph [0035], line 5 of the specification as originally filed. Thus, the trigger/stop signals are marked at the output terminal of the detecting circuit as shown in Fig. 4. Furthermore, the operational status of the first operational receiving circuit (311) of the first differential comparator (31) is detected at the spot marked "a," as shown in Fig. 4 and described on paragraph [0031], lines 3-4 of the specification as originally filed. The operational principles regarding how the detecting circuit (30) can detect the status of the first differential receiving circuit (311), and how this "a trigger signal" can activate the second differential comparator (32) are further analyzed and described as follows.

Firstly, as shown in Fig. 4 of the present invention, one with the ordinary skill in the field would know that: (a) if (In+ & In-) >2, the first differential comparator (31) works ==> the voltage level of "a" is relatively high==>(the voltage

level of the output signal from the detecting circuit (30) to the pre-amplifier receiving circuit (321)) is relatively high (a stop signal) ==> the pre-amplifier receiving circuit (321) is off; and (b) if (In+ & In-) <2, the first differential comparator (31) doesn't work ==> the voltage level of "a" is relatively low ==> (the voltage level of the output signal from the detecting circuit (30) to the pre-amplifier receiving circuit (321)) is relatively low (a trigger signal) ==> the pre-amplifier receiving circuit (321) is on. Secondly, "a stop signal" means that the voltage level of "a" is relatively high, and "a trigger signal" means that the voltage level of "a" is relatively low. Thirdly, from the above-mentioned description, the detecting circuit (30) can detect the status of the first differential receiving circuit (311) by sensing the voltage level of the marked place "a" to detect an input voltage of the detecting circuit (30) (an input signal of the detecting circuit (30)) as shown in Fig. 4 of the present invention.

Furthermore, as pointed out by the esteemed Examiner, the voltage level of the trigger/stop signals = (VDD - transistor-connected diode drop), one with the ordinary skill in the field would know that when the voltage level of "a" (as shown in Fig. 4 of the present invention) is relatively low, the voltage drop of the transistor-connected transistor T1 is relatively high, and thus the level of the output of the detecting circuit (30) (=VDD - voltage drop of T1) is relatively low (a trigger signal) firstly. Secondly, when the voltage level of "a" is relatively high, the

voltage drop of the transistor-connected transistor T1 is relatively low, and thus the level of the output of the detecting circuit (30) (=VDD - voltage drop of T1) is relatively high (a stop signal) secondly. Thus, when the voltage level of the output signal of the detecting circuit (30) is lower enough (a trigger signal), the transistor T6 of the level shift circuit (3211) would be turned on instead of always being turned off by a relatively higher positive voltage as considered by the esteemed Examiner. For the reasons set forth above, Applicants request withdrawal of the objections as well as the rejection of claim 1 under 35 U.S.C. § 112, first paragraph.

With respect to the rejection of claims 1-12 under 35 U.S.C. § 112, second paragraph, as mentioned above, claims 3, 4, 8, 10, and 11 are amended to follow the comments of the esteemed Examiner that the two transistors of the shared active load (312) are only the loads of the amplifier comprising elements (31). Besides, the answers to why the detecting circuit (30) can detect the status of the first differential comparator (31) (including elements: the first differential receiving circuit (311), and the shared active load (312)), how the "trigger signal" is produced and where it is in Fig. 4, and why the trigger signal can turn on the second differential receiving circuit (including elements: the pre-amplifier receiving circuit (321) and the main differential receiving circuit (322)) are either given in the modified Fig. 4 of the present invention, or given in the above-mentioned

description so as to clarify the indefiniteness of the claims 1-12 of the present invention.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection directed to claims 1-12.

For the above reasons, Applicants respectfully submits that the presently claimed invention is in condition for substantive examination. Reconsideration and allowance of the claims is respectfully requested.

Respectfully submitted,

Ta et al.

By_____
John C Donch Jr.
Registration No. 43,593
(215) 568-6400

Volpe and Koenig, P.C.
United Plaza, Suite 1600
30 South 17th Street
Philadelphia, PA 19103

JCD/dmr
Enclosures (4)

IN THE DRAWINGS

The "first differential comparator circuit" and "second differential comparator circuit" in Fig. 3 of the drawings of the present invention are replaced by "first differential comparator" and "second differential comparator" respectively according to the corresponding terms employed in the claims as originally filed.

All the transistors are labeled, and the numeral references of 31 and 32 as well as the trigger/stop signals are marked in Fig. 4 of the present invention to clarify the contents of the present invention as the esteemed Examiner has suggested.

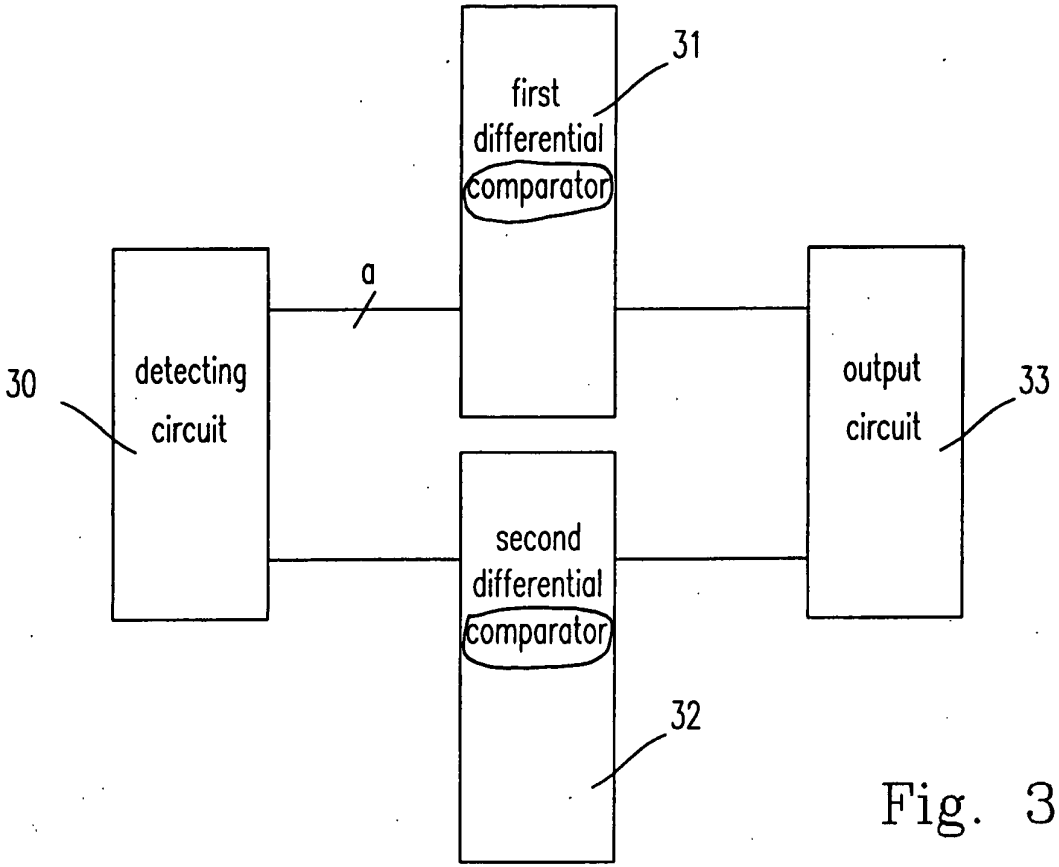
first
differential
comparator
31
a
30
detecting
circuit
output
circuit
33
second
differential
comparator
32

Fig. 3

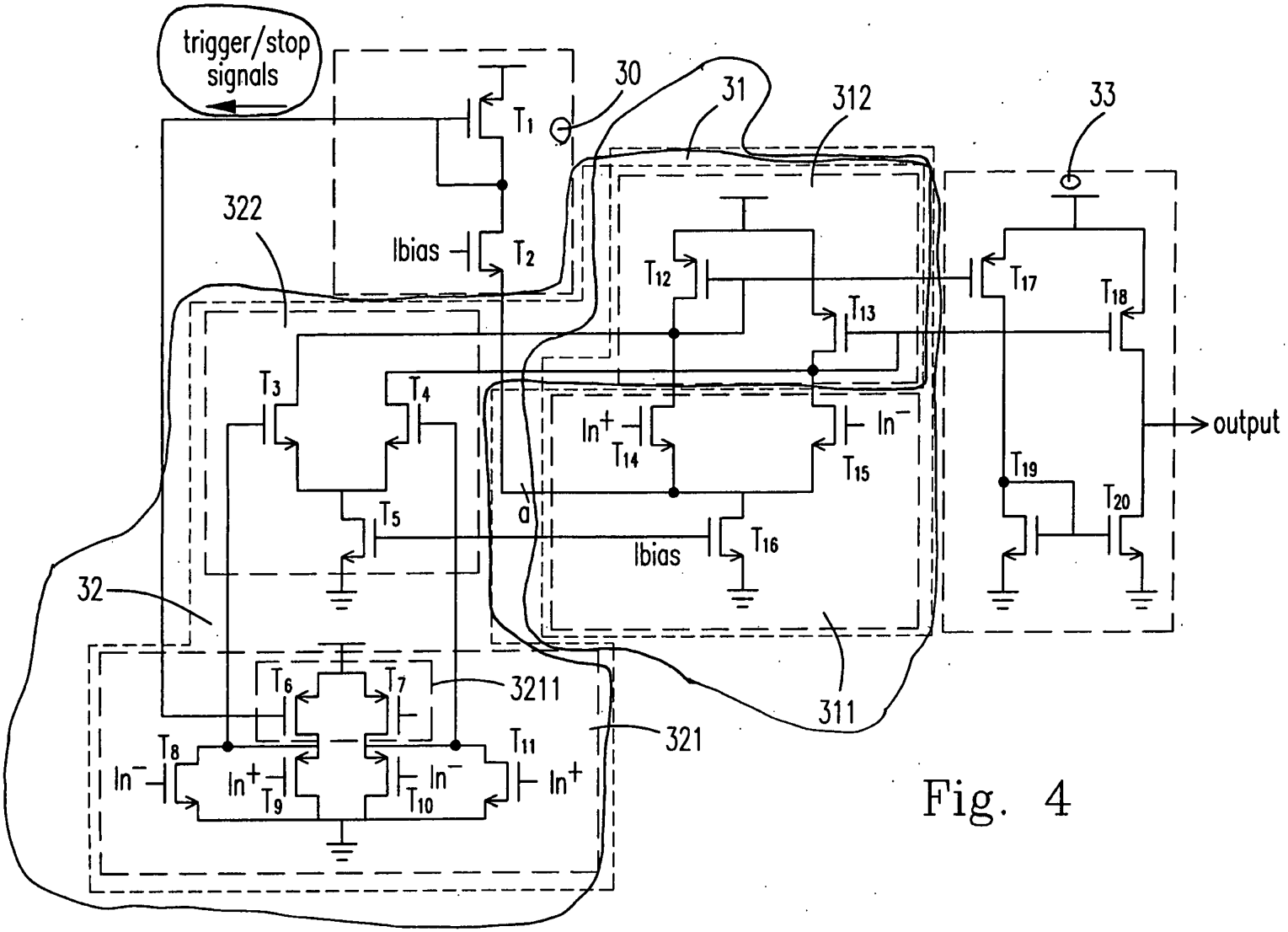
trigger/stop signals
30
31
312
33
322
Ibias
T1
T2
T12
T13
T17
T18
T3
T4
In+
In−
T14
T15
output
T19
T20
T5
a
Ibias
T16
32
T6
T7
3211
T8
T11
321
In−
In+
In+
In−
T9
T10
311

Fig. 4